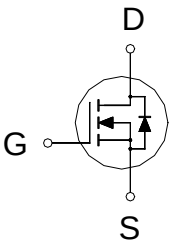
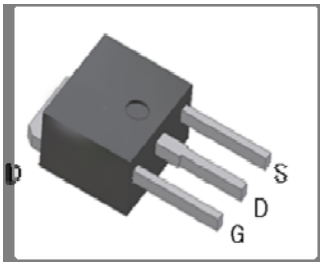
N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	100V
$R_{DSON\ (MAX.)}$	14mΩ
I_D	40A





UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	±30	V
Continuous Drain Current	T_C = 25 °C	I_D	40	A
	T_C = 100 °C		28	
Pulsed Drain Current[1]		I_{DM}	140	
Avalanche Current		I_{AS}	40	
Avalanche Energy	L = 0.1mH, ID=40A, RG=25Ω	E_{AS}	80	mJ
Repetitive Avalanche Energy[2]	L = 0.05mH	E_{AR}	40	
Power Dissipation	T_C = 25 °C	P_D	39	W
	T_C = 100 °C		15.6	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		3.2	°C / W
Junction-to-Ambient	$R_{\theta JA}$		62.5	

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle ≤ 1%

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	3.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±30V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80V, V_{GS} = 0V			1	μA
		V_{DS} = 70V, V_{GS} = 0V, T_J = 125 °C			25	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10V, V_{GS} = 10V	40			A
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 20A		12	14	mΩ
Forward Transconductance[1]	g_{fs}	V_{DS} = 5V, I_D = 20A		42		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		3330		pF
Output Capacitance	C_{oss}			200		
Reverse Transfer Capacitance	C_{rss}			43		
Gate Resistance	R_g	V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz		1.7		Ω
Total Gate Charge[1,2]	Q_g	V_{DS} = 50V, V_{GS} = 10V, I_D = 20A		39.3		nC
Gate-Source Charge[1,2]	Q_{gs}			24.3		
Gate-Drain Charge[1,2]	Q_{gd}			3.1		
Turn-On Delay Time[1,2]	$t_{d(on)}$	V_{DS} = 50V, I_D = 1A, V_{GS} = 10V, R_{GS} = 6Ω		20		nS
Rise Time[1,2]	t_r			80		
Turn-Off Delay Time[1,2]	$t_{d(off)}$			90		
Fall Time[1,2]	t_f			90		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I_S				40	A
Pulsed Current[3]	I_{SM}				140	
Forward Voltage[1]	V_{SD}	I_F = 20A, V_{GS} = 0V			1.3	V
Reverse Recovery Time	t_{rr}	I_F = 20A, dI_F/dt = 100A / μS		150		nS
Reverse Recovery Charge	Q_{rr}			450		nC

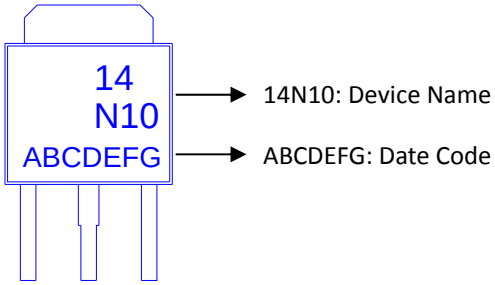
[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

[2]Independent of operating temperature.

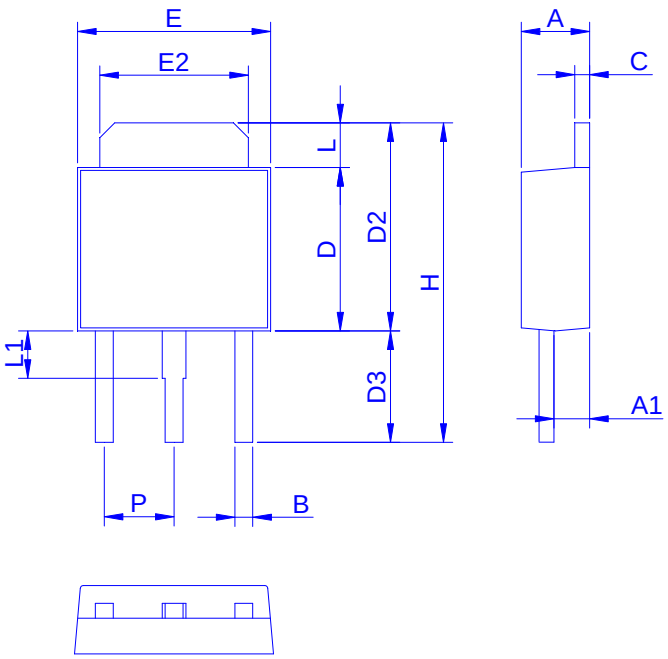
[3]Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: LB14N10E for IPAK (TO-251)



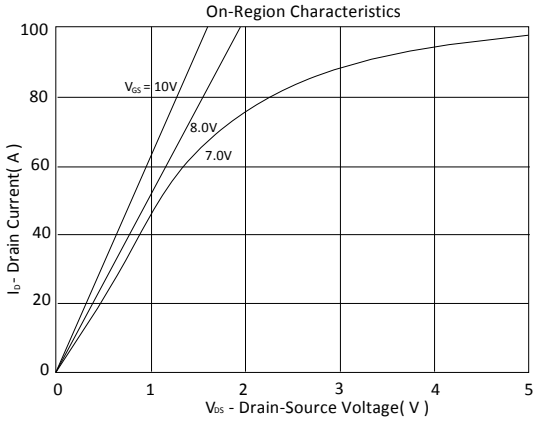
Outline Drawing

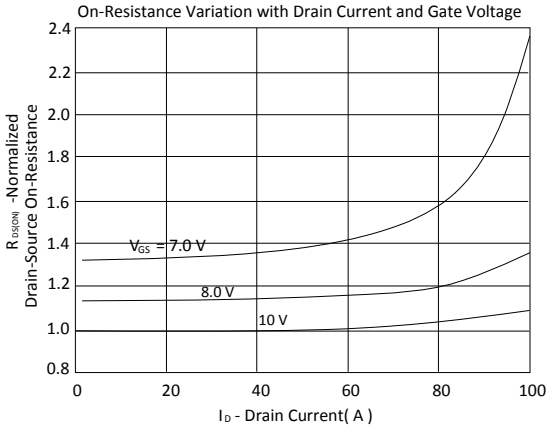


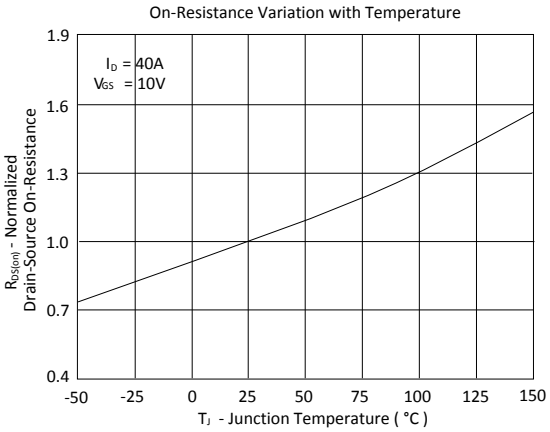
Dimension in mm

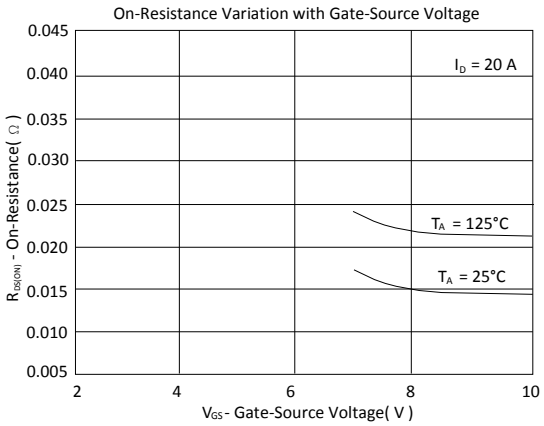
Dimension	A	A1	B	C	D	D2	D3	E	E2	H	L	L1	P
Min.	2.10	0.86	0.40	0.40	5.30	6.70	3.30	6.30	4.80	10.2	0.89	0.90	2.10
Max.	2.50	1.50	0.90	0.60	6.25	7.30	4.30	6.80	5.50	11.5	1.40	1.80	2.50

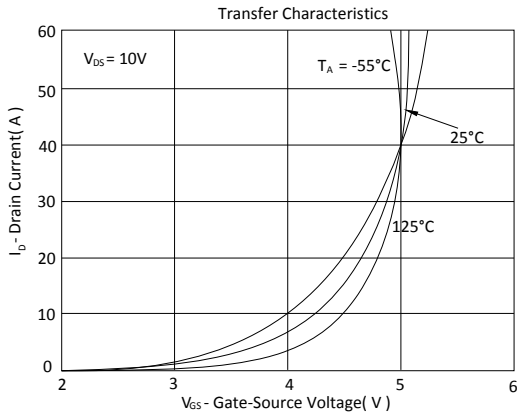
TYPICAL CHARACTERISTICS

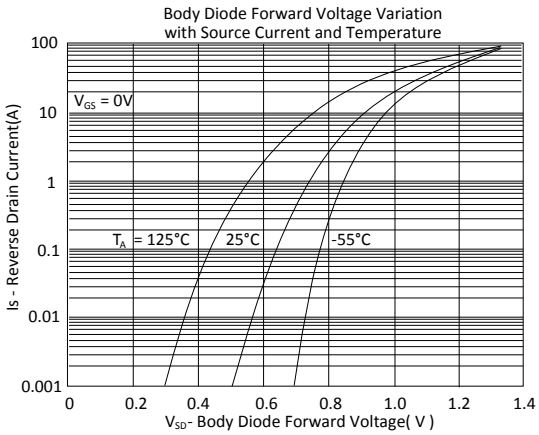




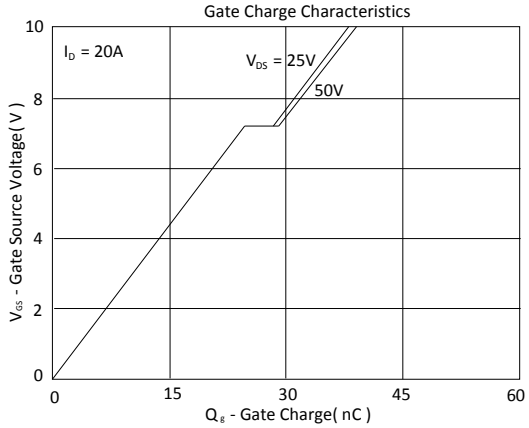




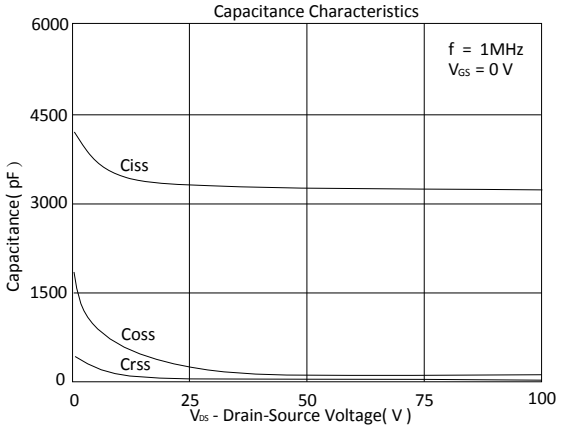




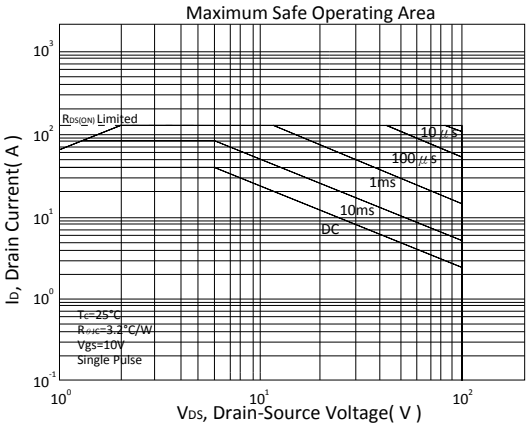
Gate Charge Characteristics



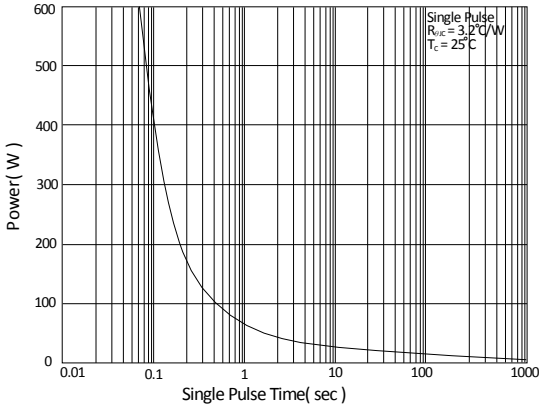
Capacitance Characteristics



Maximum Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve